IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A system comprising:

a peripheral controller comprising a core processing circuit, an internal data bus coupled to the core processing circuit, registers formed in one of a cache memory array associated with the core processing circuit and a memory coupled to the core processing circuit through the internal data bus, and at least one address translation unit coupled to the internal data bus; and

a host processing system coupled to the core processing circuit through an external data bus, the host processing system comprising:

a host bridge coupled to the external data bus;

logic to maintain the core processing circuit in a reset state during power up of the core processing circuit;

logic to initiate one or more write bus transactions at the address translation unit to load a reset vector to one or more of the registers at a boot address associated with the core processing circuit while the core processing circuit is in the reset state, the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit upon release from the reset state;

a system memory coupled to the host bridge;

logic to set the address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit, wherein the reset vector comprises at least one instruction to fetch data from the system memory via the host bridge, the address translation unit being configured to convert an internal data bus address associated with the outbound transaction to an external data bus address and configured to forward the outbound transaction from the internal data bus coupled to the core processing circuit to the external data bus coupled to the system memory via the host bridge; and

logic to initiate one or more read bus transactions at the address translation unit

addressed to the system memory in response to execution of the reset vector upon release from the reset state.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Original) The system of claim 1, wherein the host processing system further comprises logic to release the core processing circuit from the reset state in response to loading the reset vector at the boot address.

7. (Currently Amended) The system of claim_1, wherein the additional instructions comprise instructions to commence a power-on self test procedure.

8. (Previously Presented) The system of claim 7, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

9. (Currently Amended) A method comprising:

having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit;

initiating one or more write bus transactions at an address translation unit to load a reset vector to one or more registers at a boot address associated with the core processing circuit while the core processing circuit is in the reset state, wherein the reset vector is loaded to ~~a~~ the boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus, the reset vector comprising one or more instructions to fetch

additional instructions from a system memory coupled to the core processing circuit through a host bridge of the host processing system;

setting an address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit;

initiating one or more read bus transactions at the address translation unit addressed to the system memory in response to execution of the reset vector upon release of the core processing circuit from the reset state; and

in response to an outbound transaction, converting an internal bus address associated with the outbound transaction to an external data bus address and forwarding the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Original) The method of claim 9, wherein the additional instructions further comprise instructions to commence a power-on self test procedure.

14. (Original) The method of claim 13, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) An article comprising:

a storage medium comprising machine-readable instructions encoded there on for:

having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit;

initiating one or more write bus transactions at an address translation unit to load a reset vector to one or more registers at a boot address associated with the core processing circuit while the core processing circuit is in the reset state, wherein the instructions are loaded to ~~a~~ the boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of the host processing system;

releasing the core processing circuit from the reset state in response to loading the reset vector at the boot address; and

setting the address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit, the address translation unit being configured to convert an internal data bus address associated with the outbound transaction to an external data bus address and configured to forward the outbound transaction from an

internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Original) The article of claim 22, wherein the additional instructions comprise instructions to commence a power-on self test procedure.

28. (Original) The article of claim 27, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)